MSI-P563

Universal Input/Output Card

USER MANUAL

PC/104 Embedded PC Industrial I/O Series

Microcomputer Systems, Inc.
1814 Ryder Drive ·· Baton Rouge, LA 70808
Ph (225)769-2154 ·· Fax (225) 769-2155
http://www.microcomputersystems.com
E-mail:staff@microcomputersystems.com

CONTENTS

I. INTRODUCTION

The MSI-P563, shown in Fig. 1, is a general purpose I/O card designed for use with all PC/104 embedded systems. The card provides a versatile mixture of I/O functions for the designer which includes 24 TTL I/O lines, an IBM PC compatible asynchronous serial port, and three 16-bit counter/timers, as shown in the block diagram of Fig. 2. The card is designed for use in harsh environments such as those which occur in industrial applications.

A 82C55A PPI provides 24 TTL I/O lines which are programmable as ports A, B and C. Ports A and B are programmable as 8-bit groups of input or output lines. Port C is programmable two 4-bit groups of input or output lines. Provisions for implementing an interrupt driven strobed I/O mode are also included using option jumpers. A 10K pull-up resistor is connected to each I/O line for accommodating input
connections. Input connections are provided by 50-pin connector J1 which is compatible with Opto-22 type I/O.
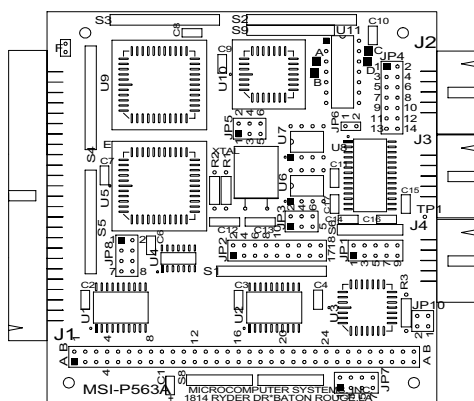

Figure 1. Card outline of the MSI-P563.

```
                          ┌──────────────────────┐                              ┌──────────────────┐
                          │      82C55A          │──────────────────────────────│     50-PIN       │
                          │  24 TTL I/O LINES    │                              │   CONNECTOR      │
                          └──────────────────────┘                              └──────────────────┘

┌──────────────┐   ┌──────────────┐   ┌──────────────┐   ┌──────────────┐      ┌──────────────────┐
│   PC/104     │   │   PC/104     │   │    16550     │   │   RS-232C    │──────│     10-PIN       │
│  8-BIT       │───│    BUS       │───│  SERIAL I/O  │───│  INTERFACE   │      │   CONNECTOR      │
│ STACKTHROUGH │   │  INTERFACE   │   │   CHANNEL    │   └──────────────┘      └──────────────────┘
│  CONNECTOR   │   └──────────────┘   └──────────────┘
└──────────────┘                                         ┌──────────────┐      ┌──────────────────┐
                                                         │  RS-422/485  │──────│     10-PIN       │
                                                         │  INTERFACE   │      │   CONNECTOR      │
                                                         └──────────────┘      └──────────────────┘

                          ┌──────────────────────┐   ┌──────────────┐          ┌──────────────────┐
                          │      82C54            │   │    CLOCK     │          │     10-PIN       │
                          │    INTERVAL          │───│    INPUT     │──────────│   CONNECTOR      │
                          │     TIMER            │   │   BUFFERS    │          └──────────────────┘
                          └──────────────────────┘   └──────────────┘
```
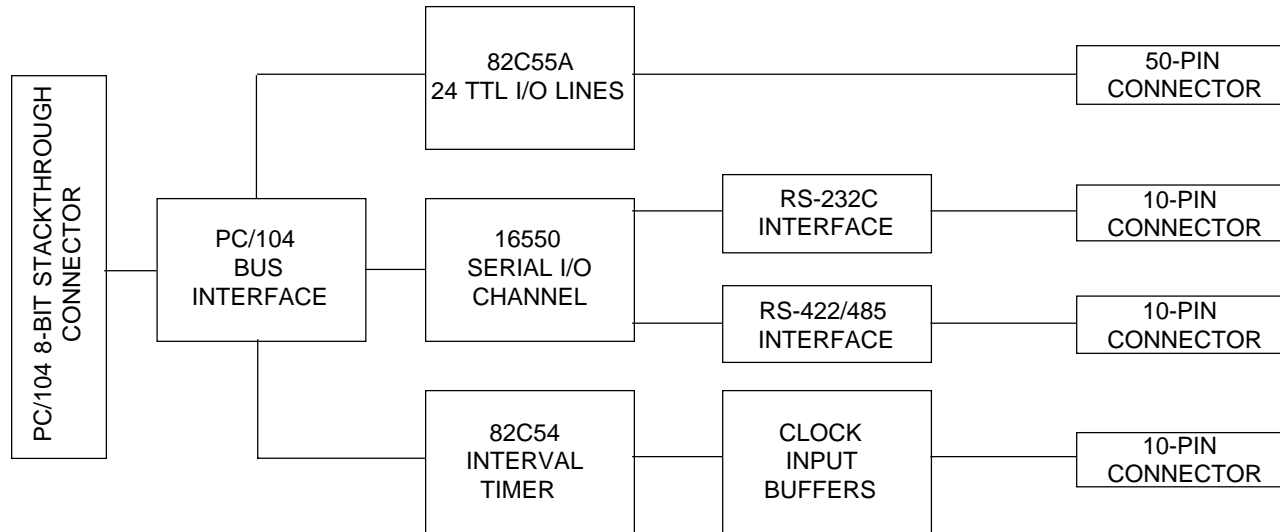
Figure 2. Block Diagram of the MSI-P563.

A 16550 UART provides a serial port that is software compatible with IBM PC software. The device is fully programmable for 5 thru 8-bit characters, selectable parity and numbers of stop bits, BAUD rates from 50 to 56K, and a selectable mode for 16-bit I/O FIFO's. The port is selectable as RS-232C, RS-422, or RS-485 using option jumpers. A hardware serial interrupt is enabled by option jumpers to select any of four interrupt-sharing channels.

The RS-232C electrical interface is generated by a MAX211E that provides RX, TX, and modem control signals CTS, RTS, DSR, DTR, RI and DCD.   Input connections are made via a 10-pin connector for a standard DTE configuration using a 10-conductor flat-cable terminated to a DE-9P type connector (omit outer conductor of flat cable from pin 10 of J3 in the DE-9E connector). The RS-422 or RS-485 electrical interface is generated by two 75163B devices that provide RX and TX. Input connections are made using a 10-pin connector J4.

A 82C54 interval timer provides three 16-bit timers programmable in six modes.   Option jumpers are provided for all gates, clock inputs and outputs of the three channels as well as the PC/104 bus signal SYSCLK (pin B20) for use to the clock inputs. All clock inputs are buffered by a socketed 74HCT00 NAND gates. The gates and buffered clock input lines are connected to 10K pull-up resistors.   External I/O connections are made via a 10-pin connector.

The card is I/O mapped using 16-bit addressing to select the various devices. The 24 TTL I/O lines of the 82C55A are jumper selectable at addresses 124H-127H on 64 distinct 1K byte boundaries. [*Note: H denotes a hexadecimal address. This notation will be used throughout the manual.*] The serial interface of the PC16550 is selectable at hex addresses for COM1 thru COM4 on 64 distinct 1K byte boundaries. The three counter/timer channels are selectable at hex addresses 120H-123H on 64 distinct 1K byte boundaries. Other addresses can be provided by MSI if required by programming of the 22CV10A device.

I. HARDWARE DESCRIPTION

A. Card Addressing

The card is I/O mapped using 16-bit addressing to select the card on any 1K-byte boundary in the address region of 0 to 0FFFFH. This address is a *base address* which is jumper selectable using option jumpers A10 thru A15 of JP2, as given in Table 1. An installed jumper sets the address value to 0. Conversely, an uninstalled jumper sets the value to 1. For example, installing JP2-1,2 and JP2-9,10 gives a base address of 7400H.

Table 1. Base address and serial I/O jumper designations.

Jumper	Address	Jumper	Address
J2-1,2	A15	J2-11,12	A10
J2-3,4	A14	J2-13,14	S1
J2-5,6	A13	J2-15,16	COMX
J2-7,8	A12	J2-17,18	COMY
J2-9,10	A11		

The *device address* is a unique address defined by the the PLD of U4. The physical address of any device is then equal to

Device Physical Address = Base Address + Device Address

Device addresses are given in Table 2. In the table, COM1, COM2, COM3 and COM4 addresses use 8 contiguous bytes with the first byte located at 3F8H, 2F8H, 3E8H and 2E8H, respectively.

Table 2. Device addresses for the MSI-P563.

Device	JP2 Jumpers	Device Address
82C55A (U10)	None	304H - 307H
16550 (U6)	None	COM1
	S1	COM1 **
	COMX	COM2
	COMX, S1	COM2 **
	COMY	COM3
	COMY, S1	COM3 **
	COMX, COMY	COM4
	COMX, COMY, S1	COM4 **
82C54 (U11)	None	300H - 303H

*** Device enabled on every 1-K Byte boundary. Enables accessing
UART at standard COMx addresses in the first 1-K Byte when a base
address is greater than 0.*

B. 82C55A Programmable Peripheral Interface

The 82C55A (U9) provides 24 TTL I/O lines via 50-pin connector
J1. The pin assignments are compatible with Opto-22 type I/O,
as given in Table 3. Ports A and B of the 82C55A can be
programmed as either input or output lines groups of eight bits
and port C can be selected as input or output lines in two groups
of 4 bits. In addition, bits 0 and 3 of port C are jumper selectable,
denoted as INTRA (JP5-2) and INTRB (JP5-4), to interrupt input
buffers (JP8-6 and JP8-8) for implementing strobed I/O on ports
A and B of the 82C55A (refer to the schematic in Appendix). Data
sheets describing the 82C55A are available on the internet at

www.okisemi.com/public/nf/Intro-6110.html

Table 3. 82C55A connector J1 pin-outs.

Pin No.	Port / Bit	Pin No.	Port / Bit
1	A / 0	27	B / 5
3	A / 1	29	B / 6
5	A / 2	31	B / 7
7	A / 3	33	C / 0
9	A / 4	35	C / 1
11	A / 5	37	C / 2
13	A / 6	39	C / 3
15	A / 7	41	C / 4
17	B / 0	43	C / 5
19	B / 1	45	C / 6
21	B / 2	49	C / 7
23	B / 3		
25	B / 4		
2-48	Ground		
50	+5V		

C. 16550 Serial Port

The 16550 (U5) provides a serial I/O port that is selectable as for RS-232C, RS-422 or RS-485 protocols. The 16550 is compatible with the UART used in the IBM PC. The interrupt output for the device (denoted as UARTINT, see schematic diagram in Appendix) is available at JP8-2 for routing to the appropriate interrupt of the PC/104 bus, as described in Section E below. Data sheets describing the 14550 are available on the internet at

www.natsemi.com/pf/PC/PC16550D.html

1. RS-232C Selection

The required jumpers for RS-232C operation are given in

Table 4. The RS-232C connector (J3) pin-outs are described in Table 5.

Table 4. Required jumpers for serial I/O.

Mode	JP3-1,2	JP3-3,4	JP3-5,6	JP6	I/O Connector
RS-232C	No	No	No	Yes	J3
RS-422 *	No	No	Yes	No	J4
RS-485 **	Yes	Yes	No	No	J4

Line termination resistors R4 (Rx) and R5 (Tx) are inserted by installing jumpers JP10-1 and JP10-2, respectively. (see schematic in Appendix).

** Transmit and receive modes are controlled by $\overline{OUT1}$ of 16550 as described in Section II.C.3. Line termination resistor R4 (Tx/Rx) is inserted by installing jumper JP10-1.

Table 5. RS-232C connector J3 pin-outs.

Pin No.	Function	Pin No.	Function
1	DCD	6	RX
2	TX	7	DTR
3	GND	8	DSR
4	RTS	9	CTS
5	RI	10	N/C

1. RS-422 Selection.

The required jumpers for RS-422 operation are given in Table 4. The RS-422 connector (J4) pin-outs are described in Table 6. If line termination resistors are required, install jumper JP10-1 to insert 120 Ohms across the transmitter output (TX) and JP10-2 for 120 Ohms across the receiver input (RX).

Table 6. RS-422 connector J4 pin-outs.

Pin No.	Function	Pin No.	Function
1	GND	6	N/C
2	FGND*	7	TX+
3	TX-	8	N/C
4	N/C	9	RX+
5	RX-	10	N/C

Incorporates a 43 Ohm series resistor to ground.

1. RS-485 Selection.

The required jumpers for RS-485 operation are given in Table 4. The RS-485 connector (J4) pin-outs are described in Table 7. If a line termination resistor is required, install jumper JP10-1 to insert 120 Ohms across the transmitter/receiver I/O (TX/RX).

The transmit and receive modes of the 16550 UART are controlled by the OUT1 pin (complement of data bit 2 of the Modem Control Register) as follows:

OUT1	Mode
0	Receive
1	Transmit

Table 7. RS-485 connector J4 pin-outs.

Pin No.	Function	Pin No.	Function
1	GND	6	N/C
2	FGND*	7	TX+/RX+
3	TX-/RX-	8	N/C
4	N/C	9	N/A
5	N/A	10	N/C

Incorporates a 43 Ohm series resistor to ground.

D. 82C54 Programmable Interval Timer

The 82C54 (U10) provides three 16-bit counters for timer/ counter operations via 10-pin connector J2. The jumpers used for configuring the 82C54 are given Table 8. The pin assignments for J2 are given in Table 9.   Data sheets describing the 82C54 are available on the internet at

www.okisemi.com/public/nf/Intro-6100.html

Table 8. Jumpers for 82C54 configuration.

Jumper	Function	Jumper	Function
JP4-1	GATE0	JP4-8	CLK2
JP4-2	CLK0	JP4-9	OUT2
JP4-3	OUT0	JP4-10	INVERT IN*
JP4-4	GATE1	JP4-11	SYSCLK**
JP4-5	CLK1	JP4-12	INVERT OUT*
JP4-6	OUT1	JP4-13	UART CLK***
JP4-7	GATE2	JP4-14	GND

Denotes a 74HCT14 inverter. Two other inverters are available using solder pads A thru D (see schematic diagram of Appendix).

*** SYSCLK is the PC/104 bus clock from pin B20.*

**** UART CLK is a 1.8432 MHz clock.*

Table 6. 82C54 connector J2 pin-outs.

Pin No.	Function	Pin No.	Function
1	GATE0	6	OUT1
2	CLK0	7	GATE2
3	OUT0	8	CLK2
4	GATE1	9	OUT2
5	CLK1	10	GND

E. Interrupt Connections

Interrupt connections to the PC/104 bus are implemented using pins 1 thru 10 of JP1, 1 thru 8 of JP7, 1 thru 6 of JP8 and 1 thru 5 of JP5, as defined in Tables 10, 11, 12 and 13, respectively. The steps in the procedure for a single interrupt, say INTx , where INTx is any one of INTR0 thru INTR3 from onboard devices (see schematic diagram in Appendix) are as follows.

1) INTx is jumpered to a single desired interrupt, IRQ4 thru IRQ9, using the appropriate pin of JP1.

2) If no other cards in the system are using the interrupt line chosen in step 1, proceed to step 3.

The tri-state buffers of U4 control the interrupt signals reaching JP1. These buffers are enabled using the jumpers of JP8. When other cards are using the same interrupt line chosen in step 1, insert the appropriate jumper for INTx. This results in the tri-state buffer of INTx being enabled only when an interrupt request is active. The status of each device is then checked to determine which interrupt is active.

3) The appropriate pin for INTx on JP7 (1 KOhm pull-down resistors) is used to properly terminate the interrupt line selected in step 1. This pin should be jumpered to the interrupt line on only one card in the system.

4) The interrupt signal from the onboard device (e.i., 82C55A, 16550 or 82C54) must be jumpered to the appropriate buffer input pin of JP5 for the INTx that was selected.

Table 10. Interrupt Jumpers for JP1.

Jumper	Function	Jumper	Function
JP1-1	IRQ7 to bus	JP1-6	INTR1 input
JP1-2	IRQ9 to bus	JP1-7	IRQ4 to bus
JP1-3	IRQ6 to bus	JP1-8	INTR3 input*
JP14	INTR2 input	JP1-9	IRQ3 to bus
JP1-5	IRQ5 to bus	JP1-10	INTR0 input

* 16550 interrupt input

Table 11. 1KOhm termination jumpers for JP7.

Jumper	Function	Jumper	Function
JP7-1,2	1K for INTR2	JP7-5,6	1K for INTR3
JP7-3,4	1K for INTR1	JP7-7,8	1K for INTR0

Table 12. Tri-state buffer enable jumpers for JP8.

Jumper	Function	Jumper	Function
JP8-1,2	INTR3 for 16550	JP8-5,6	INTR0
JP8-3,4	INTR2	JP8-7,8	INTR1

Table 13. Interrupt input jumpers for JP5.

Jumper	Function	Jumper	Function
JP5-1	INTR0 input	JP5-4	INTRB of 82C55A
JP5-2	INTRA of 82C55A	JP5-5	INTR2
JP1-3	INTR1 input	JP5-6	GND

III. SPECIFICATIONS

PC/104   8-bit, stackthrough

Digital I/O Lines
      PPI   82C55A
      Port A & B   8-bit, Input or Output
      Port C   Two 4-bit, Input or Output
      Interface   TTL levels
      Connectors One 50-pin, 0.100" grid
                (AMP 1103311-1)

Serial Channel
      UART   PC16550DV
      BAUD Rate 50 thru 56K
      Word SIze   5, 6, 7 or 8 Bits
      Stop Bits   1, 1.5, or 2
      Parity   Even, odd, or none
      Interfaces   RS-232C, RS-422/RS-485
      Control   CTS, RTS, DSR, DTR, RI
                and DCD (RS-232C)
      Connectors Two 10-pin, 0.100" grid
                (AMP 1-103311)

Counters/Timers
      Device   82C54
      Channels   Three, 6 programmable modes
      Clock Input DC to 8 MHz
      Clock Buffers 74HCT00 inverters
      Connector   10-pin, 0.100" grid
                (AMP 103311-1)

Interrupts
      Channels   Four, sharing with tri-state
                buffers for IRQ3-7, 9
Option Jumpers .025" square posts, 0.1" grid
Electrical & Environmental
     +5V @ 200 mA typical
     -40° to 85° C